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	ELECTRONIC COMPONENTS GROUP SHARP CORPORATION	REPRESENTATIVE DIVISIO
APPROVED BY: DATE 17.OCT.2006		RF DEVICES DIV.
21 19 ~	SPECIFICATION	
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	DEVICE SPECIFICATION for	
	IGITAL DBS TUNER with LINE	
MO	DEL NO. $BS2F7HZ016$	5
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SHARP			MODEL No. BS2F7HZ0165	SPEC №. EC-06X06	PAGE 2 / 17
BECOR	DS OF REVISIO	N	DOC. FIRST ISSUE 17.00	CT.2006	
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DATE	REF. PAGE PARAGRAPH DRAWING N₀.	REVISED No.	SUMMARY		CHECK & APPROVAL
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MODEL No. BS2F7HZ0165 er intended for use in Digit	SPEC No. EC-06X06	page 3/17		
is composed of 8bit ADC his tuner has DVB commo	, multistandard D	/B-S/DVB-S2		
950MHz to 2150MHz				
-65dBm to -25dBm				
F type Female				
75 ohm				
Conexant CX24118A Reference clock: Internal address: 14h	40.444MHz crystal	oscillation		
PLL synthesizer built in tuner IC "CX24118A"				
Conexant CX24116 Reference clock: 40.444MHz supplied from "CX24118A 7-bit device address: 05h 8-bit device write address: 0Ah 8-bit device read address: 0Bh				
91MHz				
 Inner Viterbi and Outer Punctured rates 1/2, 2/3 [DVB-S2] Channel symbol rates Inner LDPC and outer I 	Reed-solomon de 3, 3/4, 5/6, 6/7, 7/8 = QPSK 10 - 30MS and 8PSK 10 - 30 BCH decoding	ps,)MSps		
(B2, B3 and B4) 3.3V +/ (VDD) 1.25V +	- 0.165V DC +/- 0.060V DC			
Humidity 25 %R	H to 75 %RH			
EUROPEAN PARLIAME 27 January 2003 on the	NT AND OF THE restriction of the ι	COUNCIL of se of certain		
	950MHz to 2150MHz -65dBm to -25dBm F type Female 75 ohm Conexant CX24118A Reference clock: Internal address: 14h PLL synthesizer built in tu Conexant CX24116 Reference clock: 40.444M 7-bit device address: 05h 8-bit device write address 8-bit device read address 91MHz [DVB-S] >Channel symbol rate = >Inner Viterbi and Outer >Punctured rates 1/2, 2/ [DVB-S2] >Channel symbol rates = >Inner LDPC and outer I >Punctured rates 1/2, 3/ (B2, B3 and B4) 3.3V +/ (VDD) 1.25V - Temperature 15 deg Humidity 25 %R Period 6 mont RoHS compliant (RoHS refers to the "DII EUROPEAN PARLIAMEI 27 January 2003 on the hazardous substances	950MHz to 2150MHz -65dBm to -25dBm F type Female 75 ohm Conexant CX24118A Reference clock: Internal 40.444MHz crystal address: 14h PLL synthesizer built in tuner IC "CX24118A Conexant CX24116 Reference clock: 40.444MHz supplied from 4 7-bit device address: 05h 8-bit device write address: 0Ah 8-bit device write address: 0Ah 8-bit device read address: 0Bh 91MHz [DVB-S] >Channel symbol rate = 2 - 45MSps >Inner Viterbi and Outer Reed-solomon ded >Punctured rates 1/2, 2/3, 3/4, 5/6, 6/7, 7/8 [DVB-S2] >Channel symbol rates = QPSK 10 - 30MS and 8PSK 10 - 30 >Inner LDPC and outer BCH decoding >Punctured rates 1/2, 3/5, 2/3, 3/4, 4/5, 5/6 (B2, B3 and B4) 3.3V +/- 0.165V DC (VDD) 1.25V +/- 0.060V DC Temperature 15 deg.C to 35 deg.C Humidity 25 %RH to 75 %RH Period 6 months RoHS compliant (RoHS refers to the "DIRECTIVE 2002/95 EUROPEAN PARLIAMENT AND OF THE 27 January 2003 on the restriction of the u hazardous substances in electrical an		

		MODEL No. BS2F7HZ0165	SPEC No. EC-06X06	PAGE 4/17		
SHARP						
Before handling the unit from Ele 2) Avoid following a) to store this	this unit, ground ectronic Static De actions;	of the high temperature and	desks and equipme			
[2]MECHANICAL SPECIF 2-1. Dimension and more		see section [14]				
2-2. Mass		44g (typical)				
2-3. Strength of F-conne	ector	No severe transform or distortion at bending moment, 0.98N·m. To be connected electrically.				
2-4. Clamp Torque of F-	connector	No severe transform or distortion on the connection with F-connector at bending moment, 0.98N · m. To be connected electrically.				
[3] ENVIRONMENTAL SP (ELECTRICAL FUNCTIO 3-1. Operating		N GUARANTEE) 0deg.C to +60deg.C Less than 85% No condensation				
3-2. Storage	Temperature Humidity	-20deg.C to +85deg.C Less than 95% Water vapor pressure 6643Pa max, without condensatio				
<notice> Please be careful th and such condensation</notice>		erature changes may cause rosion.	condensation duri	ng storage,		
[4] ABSOLUTE MAXIMUN	I VOLTAGE		Noto			

Pin name	Pin No.	MIN.	MAX	UNIT	Note
B1B	1		25	V	400mA max.
B1A	2		25	V	400mA max.
B4	3	-0.3	3.63	V	
B2	4	-0.3	3.6	V	
B3	11	-0.5	4.6	V	
VDD	13	-	1.8	V _	
SDA, SCL, RESETB	8, 9, 26	-0.5	B3+0.3	V	

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[5] TESTING CONDITION

5-1. Supply voltage

J-1. Oupply vollage						
Pin name	Pin No.	MIN.	TYP.	MAX.	UNIT	Note
B4	3	3.25	3.30	3.35	V	
B2	4	3.25	3.30	3.35		
B3	11	3.25	3.30	3.35	V.	
VDD	13	1.23	1.25	1.27	V	

65%

5-2. Ambient temperature

25deg.C +/- 5deg.C

5-3. Ambient humidity

% +/- 10%

[6] ELE	ECTRICAL SPEC	CIFICATION	(Unless	otherwis	e stated t	esting co	ndition 5-1~5-3.)		
No.	lte	em	Specification			Specifi			Condition
			MIN.	TYP.	MAX.	UNIT			
6-1	RF input VSWR			2.0	2.5		950MHz to 2150MHz		
6-2	RF output VSW	R		2.0	2.5				
6-3	RF output gain		-5	0	+5	dB			
6-4	L.O. leak at inpu	it terminal		-80	-70	dBm	950MHz to 2150MHz		
6-5	PLL synthesizer	tuning time		1	5	ms	limited to CX24118A		
6-6	Symbol rate	DVB-S2/QPSK	10		30	MS/s			
		DVB-S2/8PSK	10		30	MS/s			
		DVB-S/QPSK	2		45	MS/s			
		DTV Legacy		20		MS/s	· · · · · · · · · · · · · · · · · · ·		
6-7	Carrier acquisiti	on range			+/-10	MHz			
6-8	Current	B2		160	240	mA	3.3V		
		B3		220	265	mA	3.3V		
	consumption	B4		25	40	mA	3.3V		
		VDD			1842	mA	1.25V		

[7] ERROR RATE PERFORMANCE

Es/No performance at Quasi Error Free

Mode	ETSI Ideal	Performance	Unit	Note
		(Typical)		
QPSK 1/2	1.00	1.2		>DVB-S2
QPSK 3/5	2.23	2.4		>Pilot: ON
QPSK 2/3	3.10	3.2		>BW = Synbol_rate
QPSK 3/4	4.03	4.2		>BERTester: SFU
QPSK 4/5	4.68	4.8		
QPSK 5/6	5.18	5.3		
QPSK 8/9	6.20	6.4	dB	
QPSK 9/10	6.42	6.6	UD UD	
8PSK 3/5	5.50	5.8		
8PSK 2/3	6.62	6.8		
8PSK 3/4	7.91	8.1		
8PSK 5/6	9.35	9.6		
8PSK 8/9	10.69	10.9	j	
8PSK 9/10	10.98	11.3		

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[8] SERIAL PROGRAMMING INTERFACE

8-1. Interface Control

This tuner's control interface is a 400 kHz two wire serial programming interface, as following figure. The primary means of controlling the tuner is through the firmware, with no access from the host processor. This tuner is supported using this method.



On the other hand, when the firmware is not used, tuner pass-through can be used. Following figure illustrates the tuner control interface in pass-through mode. To enable pass-through mode, write 0x55 to register field TUNI2CRptEn[7:0] (0xE9[7:0]). This will connect the main serial programming interface to the tuner bus. When a stop condition is issued by the master, serial programming interface pass-through is automatically disabled. The following examples illustrate how to use tuner serial programming interface pass-through.

Tuner Control Interface (Pass-through)

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8-1-1. Tuner Pass-through Write Procedure

- 1. Send the start condition.
- 2. Send the CX24116's address with the read/write bit low (write), and receive an ACK.
- 3. Send address 0xE9, and receive an ACK.
- 4. Send 0x55 to TUNI2CRptEn[7:0] (0xE9[7:0]) and receive an ACK. - Pass-through is now enabled.
- 5. Send a repeat-start condition.
- 6. Send the tuner's address with the read/write bit low (write), and receive an ACK. - 0x28 or 0xA8 for the CX24118A tuner.
- 7. Send the tuner register address of interest, and receive an ACK.
- 8. Send one byte of data, and receive an ACK.
- 9. Step 7 can be repeated for multiple bytes in subsequent registers.
- 10. Send a stop condition.
 - When a stop condition is issued by the master, the CX24116 disables serial programming interface pass-through.

8-1-2. Tuner Pass-through Read Procedure

- 1. Send the start condition.
- 2. Send the CX24116's address with the read/write bit low (write), and receive an ACK.
- 3. Send address 0xE9, and receive an ACK.
- 4. Send 0x55 to TUNI2CRptEn[7:0] (0xE9[7:0]), and receive an ACK. - Pass-through is now enabled.
- 5. Send a repeat-start condition.
- 6. Send the tuner's address with the read/write bit low (write), and receive an ACK. - 0x28 or 0xA8 for the CX24118A tuner.
- 7. Send the tuner register address of interest, and receive an ACK.
- 8. Send a repeat-start condition.

- It is critical that a repeat-start condition is sent at this point instead of separate stop and start conditions, because the CX24116 disables serial programming interface pass-through when a stop condition is detected.

9. Send the tuner's address with the read/write bit high (read), and receive an ACK - 0x29 or 0xA9 for the CX24118A tuners.

- 10. Receive a byte from the desired register and transmit an ACK.
- 11. Step 9 can be repeated for multiple bytes in subsequent registers.
- 12. Transmit a stop condition.
 - When a stop condition is issued by the master, the CX24116 disables serial programming interface pass-through.

Note) Please refer to the CX24116 and CX24118A Data Sheet for details of the programming.

No.	Item		Specif	Condition		
		MIN.	TYP.	MAX.	UNIT	
8-1	Low-level input voltage: V _{iL}			0.8	V	All digital inputs
8-2	High-level input voltage: V _{IH}	2.0			V	All digital inputs
8-3	High-level output voltage: V _{OH}	2.4			V	All digital outputs
8-4	Low-level output voltage: VoL			0.4	V	All digital outputs

8.2 Digital Interface Specifications

Note) Applied to not only serial programming interface but also all digital I/O pins.

8-3. Serial Programming Interface Restrictions

For robust serial programming interface operation, care should be taken to avoid short glitches on the clock and data lines. A short glitch is a voltage transition from low to high to low (0 to 1 to 0) in less than 75 ns.

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SHARP		0021111201			
[9] MPEG OUTPUT	TIMINO				
9-1. MPEG OUTPUT					
DATA TIMING	DEFINITION		MIN.	UNITS	
CPP	Clock period in parallel mode.		100.00		
CRDS	Setup time, data to clock rise.		45.75		
CRDH	Hold time, clock rise to data.		49.66		
CIFDS	Setup time, data to inverted cloc		45.19		
CIFDH	Hold time, inverted clock fall to d		50.10		
CAFDS	Setup time, data to advanced clo Hold time, advanced clock fall to		82.69 12.60	ns	
CAFDH CARDS	Setup time, data to advanced clock fail to		33.24		
CARDH	Hold time, advanced clock rise to		62.16		
CAIRDS	Setup time, data to advanced inv		83.24		
CAIRDH	Hold time, advanced inverted clo		12.16		
CAIFDS	Setup time, data to advanced inv	verted clock fall.	32.69		
CAIFDH	Hold time, advanced inverted clo	ock fall to data.	62.60		
	CPP				
RS_CLK					
			CRDS CRDS	CRDH	
		· · ·	1		Normal Clock
RS_DATA[7:0]	X d0 X d1	<u> </u>	<u>X d1</u>	187 X	ue.
RS_CLK				Г	
	II				
					Inverted Clock
DO DATAI7.01	1b X 0b X		• • •	187 X	invented Olock
RS_DATA[7:0]	X d0 X d1		<u> </u>		
RS_CLK		ר=ח ר			
	CAFDS CAFDH	 C	ARDSC	ARDH	- Advanced
			J~~	······································	Normal Clock
RS_DATA[7:0]	X d0 X d1	X	X d'	187 🕺	Normal Olook
					~
		ii		r	
RS_CLK		<u>_</u>			.
	CAIRDS	C	AIFDS		Advanced
RS_DATA[7:0]			V A-	187 X	Inverted Clock
		<u> </u>	<u> </u>		*
		•			

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SHARP					
9-2. MPEG Serial	Output Mode				
DATA TIMING	DEFINITION	· • • • • • • • • • • • • • • • • • • •	MIN.	UNITS	
CPS	Clock period in serial mode.		100.00		
CFDSS	Setup time, data to clock fall.				
CFDHS	Hold time, clock fall to data.				
CRDSS	Setup time, data to clock rise.				
CRDHS	Hold time, clock rise to data.				
CIRDSS	Setup time, data to inverted cloc	k rise.			
CIRDHS	Hold time, inverted clock rise to				
CIFDSS	Setup time, data to inverted cloc	k fall.			
CIFDHS	Hold time, inverted clock fall to c	lata.		·	
	~ D ^				
	CPS				
<u>RS_CLK</u>					
	CFDSS CFDHS CFL	OSS CRDHS			
					Normal Clock
RS_DATA0	χ d0 χ d1 χ d2 χ d3 χ d	14 X d5 X d6 Xd	7 <u>X</u> 88 Xd	aVanV	
RS_CLK					
		DSS CIFDHS			
					Inverted Clock
RS_DATA0	$\times d0 \times d1 \times d2 \times d3 \times d3$	14 X d5 X d6 Xd	7X d8Xd	9Xd10X	

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8	SHARP			
•	 [10] Reliability 10-1. High temperature high humidity load (4 1) After leaving DUT at room temperature a value. 2) After cycling DUT in the constant ch leave the DUT at room temperature a 3) Must meet the specifications of Table 4) The contact resistance of F-connector 	ature and humidity for a namber at 40deg.C/90-9 and humidity for 2h and a 10-2.	24h or longer, mea 95% RH in on state, then measure value	for total 500h,
	 High temperature load (70deg.C, 40% After leaving DUT at room temperature. After leaving DUT in the constant of DUT at room temperature and humid Must meet the specifications of Table 	ature and humidity for hamber at 70+/-2deg.C lity for 2h and then mea	/40% RH for total 5	500h, leave the
	 10-3. Cold test (-25deg.C, 500h) 1) After leaving DUT at room temperatvalue. 2) After leaving DUT in the constant teat room temperature and humidity for 3) Must meet the specifications of Table 	mperature chamber at r 2h and then measure	-25deg.C for 500h,	leave the DUT
	 Shock (686 m/s², 6 planes, 3 times) After leaving DUT at room tempera values. Using the shock tester, apply shocl measure the values. Must meet the specifications of Table 4) This test is to be conducted using a set of the state of the s	k of 686 m/s ² three tim e 10-2.		
	 10-5. Vibration (10-55 Hz, 1.5 mm, in each of 1) After leaving DUT at room temperativalues. 2) Using the vibration tester, apply refrequency being varied uniformly being unitally perpendicular directions (X, 3) Must meet the specifications of Table 4) This test is to be conducted using a set of the specification of th	ature and humidity for motion having an amp etween 10 and 55 Hz, Y and Z, total of 6h). A e 10-2.	24h or longer, mea plitude of 1.5 mm , to DUT, for 2h in	sure the initial (constant), the each of three
	 Heat shock test (1 cycle=1h (-20deg.C) After leaving DUT at room temperatu Using the heat shock tester, apply he Must meet the specifications of Table The contact resistance of F-connector 	ure and humidity for 24h eat shock to DUT. After e 10-2.	or longer, measure the test, measure th	
	10-7. Solderability of terminal Pretreatment of heating terminal at temperature for 2h or longer. Immerse 1. rosin (JIS-K-5902), isopropyl alcohol (range) approx. 25% by weight unless oth immerse the length of the terminal into a 240 +/-2deg.C for 3s.Dipped terminal po cutting plane of the chassis)	9 mm length of termina JIS-K-8839 or JIS-K-1 erwise specified) or equation pool of molten solder	al (from the tip) to b 522, rosin concent uivalent solution for (Sn/3.0Ag/0.5Cu, o	e soldered into ration (10-35% 3–5s, and then r equivalent) at

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10-8. Soldering heat resistance

Immerse the terminal mounted on a PCB (1.6t thick) into solder at 350±5deg.C for 3.0-3.5 seconds or at 260 +/-5deg.C for 10 +/-1 seconds. Remove the PCB from the solder and leave it for 1 hour at room temperature. The test sample shall show no degradation in appearance and electrical characteristics.

10-9. ESD protection

Table 10-1; ESD Test Condition (IEC61000-4-2 Compliant)

Terminal	Limits	Condition
RF_IN (coaxial center)	+/-6kV DC	150pF/330ohm each 5 times
Others	+/-200V DC	150pF/330ohm each 5 times

Table 10-2

No.	Item		Spec.	UNIT	Condition
10-1	Current	B2	< 240	mA	3.3V
	consumption	B3	< 265	mA	3.3V
		B4	< 40	mA	3.3V
		VDD	< 1842	mA	1.25V
10-2	Es/No at QEF	8PSK 3/4	< 8.2	dB	DVB-S2, Pilot: ON

(*)Method of measuring contact resistance

Center-contact

Insert the gauge $pin(\varphi 0.8mm)$ to F-connector.

Measure the resistance between the gauge and the center-contact of F-connector. Outer-shell

Connect the plug(3/8-32 UNEF-2B) to F-connector at 29.4N·cm of the clamping torque. Measure the resistance between the plug and chassis.

(Measuring device: Milliohm meter)



MODEL No.
BS2F7HZ0165

[12] F	NN L	IST

[12] PIN L	IST			
No.	NAME	Logic	PIN DESCRIPTION	
1	B1B		Voltage supply for LNB B. Please ground it with a 1000pF ceramic capacitor.	
2	B1A		Voltage supply for LNB A. Please ground it with a 1000pF ceramic capacitor.	
3	B4		3.3V supply for Booster Amp. within this module.	
4	B2		3.3V supply for CX24118A tuner IC.	
5,6,7,10	NC		It is not connected inside the unit. We advice to ground it.	
8	SDA	3.3V	Serial programming interface data. Please connect a pull-up resistor which is more than 2k ohm outside of the tuner.	
9	SCL	3.3V	Serial programming interface clock. Please connect a pull-up resistor which is more than 2k ohm outside of the tuner.	
11	B3		3.3V supply for CX24116 demodulator IC.	
12	LNB_22k_ Tx	3.3V	LNB tone transmit signal. Output only. DiSEqC modulated/unmodulated tone burst or continuous tone can be selected.	
13	VDD		1.25V supply for CX24116 demodulator IC. Note1)	
14,,21	RS_DATA [7;0]	3.3V	MPEG data interface data pins. In serial mode, data can be produced on RS_DATA[0] or RS_DATA[7].	
22	RS_CLK	3.3V	MPEG data interface clock pin.	
23	RS_VALID	3.3V	MPEG data interface control signal - VALID.	
24	RS_START	3.3V	MPEG data interface control signal - START.	
25	RS_FAIL	3.3V	MPEG data interface control signal - FAIL.	
26	RESET	3.3V	CX24116 chip reset. Active low. Internally pulled up. Note2)	

Note 1)

Care should be taken to ensure that current fluctuations do not cause the voltage to go outside of the voltage operating condition requirement of 1.25 V ±5 percent. To achieve this, it is recommended that a 1000uF capacitor be placed near the 1.25 V voltage regulator and that several 1 uF capacitors be placed near VDD pins. Trace impedance between the regulator and the tuner should also be kept to a minimum; ideally a power plane should be used.

Note 2)

RESET pin should be held low until after both power supplies (B3 and VDD) have been brought up. Minimum pulse duration is 10us.







