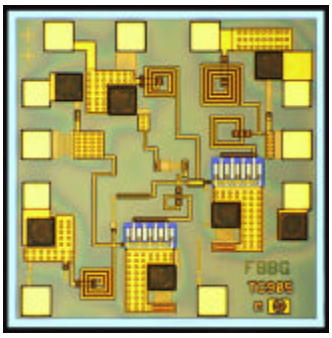
Agilent HMMC-5618

6–20 GHz Medium Power Amplifier

Data Sheet



Chip Size:	920 × 920 µm (36.2 × 36.2 mils)
Chip Size Tolerance:	± 10 µm (± 0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 × 80 µm (3.2 × 3.2 mils)

Features

- **High Efficiency: 11% @ P_{-1dB} Typical**
- **Output Power, P_{-1dB}: 18 dBm Typical**
- **High Gain: 14 dB Typical**
- **Flat Gain Response: ± 0.5 dB Typical**
- **Low Input / Output VSWR: <1.7:1 Typical**
- **Single Supply Bias: 5 volts (@ 115 mA typ.) with Optional Gate Bias**

Description

The HMMC-5618 6–20 GHz MMIC is an efficient two–stage medium-power amplifier that is designed to be used as a cascadable intermediate gain block for EW applications. In communication systems, it can be used as an amplifier for a local oscillator or as a transmit amplifier. It is fabricated using a PHEMT integrated circuit structure that provides exceptional efficiency and flat gain performance. During typical operation, with a single 5–volt DC power supply, each gain stage is biased for Class–A operation for optimal power output with minimal distortion. The RF input and RF output has matching circuitry for use in 50 ohm environments.

The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs.

Absolute Maximum Ratings[1]

Symbol	Parameters / Conditions	Min.	Max.	Units
V_{D1},V_{D2}	Drain Supply Voltage		5.5	Volts
V_{G1}	Optional Gate Supply Voltage	–5	+1	Volts
V_{G2}	Optional Gate Supply Voltage	–10	+1	Volts
I_{D1}	Drain Supply Current		70	mA
I_{D2}	Drain Supply Current		84	mA
P_{in}	RF Input Power[2]		20	dBm
T_{ch}	Channel Temperature[3]		160	°C
T_A	Backside Ambient Temperature	–55	+100	°C
T_{st}	Storage Temperature	–65	+150	°C
T_{max}	Max. Assembly Temperature		300	°C

Notes:

1. Absolute maximum ratings for continuous operation unless otherwise noted.
2. Operating at this power level for extended (continuous) periods is not recommended.
3. Refer to DC Specifications / Physical Properties table for de–rating information.

DC Specifications / Physical Properties[1]

Symbol	Parameters / Conditions	Min.	Typ.	Max.	Units
V_{D1},V_{D2}	Drain Supply Voltage	3.0	5.0	5.5	Volts
I_{D1}	Stage–One Drain Supply Current (V_{D1}=5V, V_{G1}=Open or Ground)		50		mA
I_{D2}	Stage–Two Drain Supply Current (V_{D2}=5V, V_{G2}=Open or Ground)		65		mA
I_{D1}+I_{D2}	Total Drain Supply Current (V_{D1}=V_{D2}=5V, V_{G1}=V_{G2}=Open or Ground)		115	140	mA
V_{P1}	Optional Input–Stage Gate Supply Pinch–off Voltage (V_{D1}=5V, I_{D1} < 3 mA: Input Stage OFF[2])	–4	–2.8		Volts
I_{G1}	Gate Supply Current (Input Stage OFF[2])		0.9		mA
V_{P2}	Optional Output–Stage Gate Supply Pinch–off Voltage (V_{D2}=5V, I_{D2} < 3.6 mA: Output Stage OFF[2])	–7.5	–5.3		Volts
I_{G2}	Gate Supply Current (Output Stage OFF[2])		1.7		mA
$\theta_{ch\text{-}bs}$	Thermal Resistance[3] (Channel–to–Backside at T_{ch}= 50°C)		87		°C / Watt
T_{ch}	Channel Temperature[4] (T_A=100°C, MTTF=10^6 hrs, (V_{D1}=V_{D2}=5V, V_{G1}=V_{G2}=Open)		150		°C

Notes:

1. Backside ambient operating temperature T_A = 25°C unless otherwise noted.
2. The specified FET stage is in the OFF state when biased with a gate voltage level that is sufficient to pinch off the drain current.
3. Thermal resistance (in °C / Watt) at a channel temperature T(°C) can be *estimated* using the equation:
   $\theta(T) \cong 87 \times [T(°C)+273] / [150°C+273]$.
4. De–rate MTTF by a factor of two for every 8°C above T_{ch}.

RF Specifications

(T_A=25°C, V_{D1}=V_{D2}=5V, V_{G1}=V_{G2}=Open or Ground, Z_0=50Ω)

Symbol	Parameters / Conditions	Typ.	6–18 GHz		5.9–20 GHz		Units
			Min.	Max.	Min.	Max.	
Gain	Small Signal Gain	14	12		11.5		dB
Δ Gain	Gain flatness	±0.5					dB
$\Delta S_{21} / \Delta T$	Temperature Coefficient of Gain	–0.025					dB / °C
$(RL_{in})_{MIN}$	Minimum Input Return Loss	12	10		9		dB
$(RL_{out})_{MIN}$	Minimum Output Return Loss	12	10		10		dB
Isolation	Reverse Isolation	40					dB
P_{-1dB}	Output Power at 1dB Gain Compression	18	17		17		dBm
P_{SAT}	Saturated Output Power (P_{in}=10 dBm)	20	18.5		18.5		dBm
NF	Noise Figure	5.5		7		7	dB

Applications

The HMMC-5618 is a GaAs MMIC medium-power amplifier designed for optimum Class–A efficiency and flat gain performance from 6 GHz to 20 GHz. It has applications as a cascadable gain stage for EW amplifier, buffer stages, LO–port driver, phased–array radar, and transmitter amplifiers used in commercial communication systems. The MMIC solution is a cost effective alternative to hybrid assemblies.

Biasing and Operation

The MMIC amplifier is normally biased with a single positive drain supply connected to both V_{D1} and V_{D2} bond pads as shown in Figure 10. The recommended drain supply voltage is 3 to 5 volts. If desired, the first stage drain bonding pad can be biased separately to provide a small amount of gain slope control or bandwidth extension as demonstrated in Figure 2.

No ground wires are required because all ground connections are made with plated through-holes to the backside of the device.

Gate bias pads (V_{G1} and V_{G2}) are also provided to allow adjustments in gain, RF output power, and DC power dissipation, if necessary. No connection to the gate pads is needed for single drain-bias operation. However, for custom applications, the DC current flowing through the input and/or output gain stage may be adjusted by applying a voltage to the gate bias pad(s) as shown in Figure 10b. A negative gate-pad voltage will decrease the drain current. The gate–pad voltage is approximately zero volts during operation with no DC gate supply. Refer to the Absolute Maximum Ratings table for allowed DC and thermal conditions.

Assembly Techniques

It is recommended that the RF input, RF output, and DC supply connections be made using 0.7 mil diameter gold wire. The device has been designed so that optimum performance is realized when the RF input and RF output bond–wire inductance is approximately 0.2 nH(‘0 mils) as demonstrated in Figures 4, 6, and 7.

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Additional References:

AN #49, "HMMC-5618 (6–20 GHz) Amplifier" and PN #14, "HMMC-5618 Driven by an HMMC-5020."

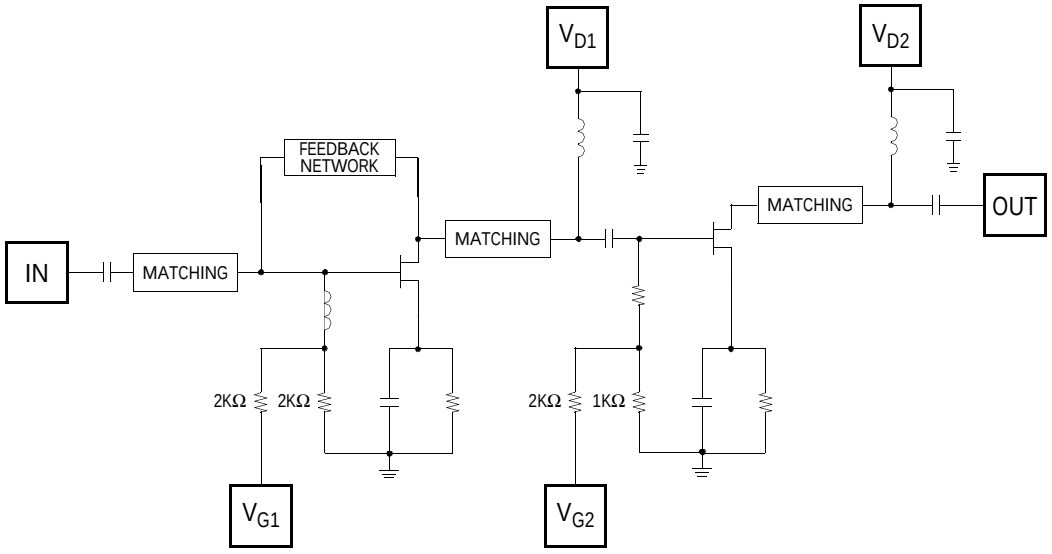


Figure 1.
Simplified Schematic Diagram

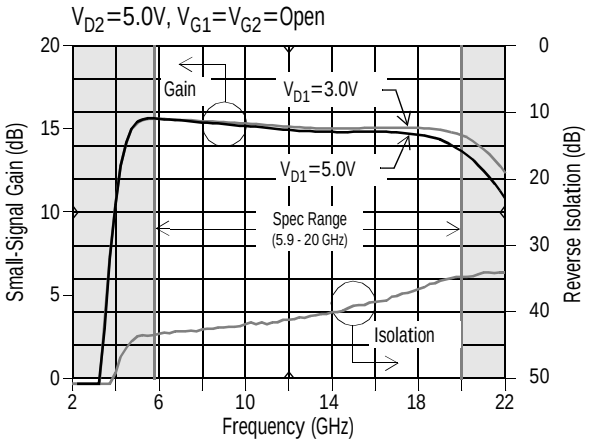


Figure 2.
Gain and Isolation versus Frequency

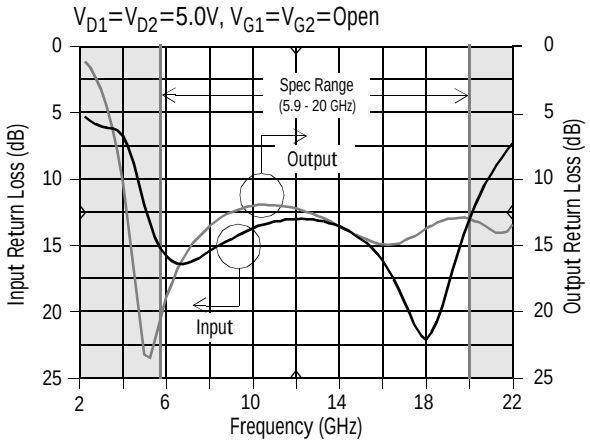


Figure 3.
Input and Output Return Loss versus Frequency

S–Parameters[1] (T_A = 25°C, V_{D1} = V_{D2} = 5.0V, V_{G1} = V_{G2} = Open, Z_o = 50Ω)

Freq. (GHz)	S_{11}			S_{12}			S_{21}			S_{22}		
	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2.0	–4.8	0.574	–140.8	–71.2	0.000	–73.5	–43.0	0.0070	117.3	–0.9	0.901	–75.4
2.5	–5.6	0.526	–166.9	–74.4	0.000	–12.0	–25.3	0.0544	–113.7	–1.6	0.835	–99.7
3.0	–6.0	0.501	166.4	–73.6	0.000	–41.3	–8.0	0.3981	–124.1	–3.3	0.687	–127.0
3.5	–6.2	0.492	136.2	–55.9	0.002	–51.8	2.9	1.4008	–159.1	–6.1	0.498	–156.7
4.0	–6.7	0.461	99.3	–49.4	0.003	–94.9	10.4	3.3208	154.4	–10.3	0.305	171.1
4.5	–8.8	0.363	60.6	–45.5	0.005	–140.6	14.2	5.1331	104.5	–16.7	0.147	133.8
5.0	–11.9	0.255	30.7	–43.8	0.006	–179.4	15.4	5.9052	62.9	–23.2	0.069	76.1
5.5	–14.4	0.190	10.9	–43.8	0.006	152.8	15.6	6.0539	31.6	–22.0	0.079	21.3
6.0	–15.8	0.163	–3.8	–43.4	0.007	132.6	15.6	6.0319	6.8	–18.9	0.114	–5.5
6.5	–16.4	0.152	–16.2	–43.4	0.007	116.8	15.6	6.0062	–14.1	–16.8	0.144	–19.6
7.0	–16.3	0.153	–27.4	–43.1	0.007	101.8	15.5	5.9669	–32.7	–15.4	0.171	–30.5
7.5	–16.0	0.159	–38.0	–43.0	0.007	87.6	15.5	5.9318	–49.7	–14.3	0.193	–39.4
8.0	–15.4	0.171	–48.2	–42.8	0.007	79.1	15.4	5.8635	–65.4	–13.5	0.212	–47.1
8.5	–14.9	0.180	–58.5	–42.7	0.007	68.9	15.4	5.8567	–80.0	–12.9	0.227	–54.4
9.0	–14.5	0.189	–67.5	–42.5	0.008	58.9	15.3	5.8232	–94.2	–12.5	0.237	–61.4
9.5	–14.1	0.198	–75.8	–42.3	0.008	50.2	15.2	5.7757	–107.8	–12.2	0.246	–67.8
10.0	–13.7	0.206	–83.6	–42.0	0.008	41.0	15.2	5.7385	–121.0	–12.0	0.252	–73.9
10.5	–13.4	0.214	–91.2	–42.0	0.008	33.7	15.1	5.7043	–133.8	–11.9	0.254	–79.6
11.0	–13.2	0.219	–98.3	–42.0	0.008	27.5	15.1	5.6618	–146.2	–11.9	0.253	–85.2
11.5	–13.0	0.223	–105.1	–41.7	0.008	19.8	15.0	5.6180	–158.4	–12.0	0.250	–90.0
12.0	–13.0	0.224	–111.4	–41.3	0.009	13.9	14.9	5.5801	–170.4	–12.2	0.245	–94.3
12.5	–13.0	0.224	–117.5	–40.9	0.009	6.2	14.9	5.5525	177.7	–12.5	0.238	–98.2
13.0	–13.1	0.221	–123.2	–40.8	0.009	1.0	14.9	5.5276	166.0	–12.8	0.230	–101.6
13.5	–13.3	0.217	–128.7	–40.5	0.009	–6.7	14.8	5.5138	154.2	–13.1	0.221	–104.3
14.0	–13.5	0.210	–134.1	–40.2	0.010	–12.5	14.8	5.5069	142.3	–13.5	0.211	–106.2
14.5	–13.9	0.201	–138.9	–40.0	0.010	–17.5	14.8	5.4997	130.5	–13.9	0.201	–107.1
15.0	–14.5	0.188	–143.4	–39.2	0.011	–25.3	14.8	5.5050	118.6	–14.4	0.191	–106.8
15.5	–15.2	0.174	–147.2	–39.1	0.011	–31.8	14.8	5.5089	106.3	–14.7	0.184	–105.4
16.0	–16.2	0.155	–150.0	–38.6	0.012	–38.9	14.8	5.5103	93.8	–14.9	0.180	–103.4
16.5	–17.5	0.133	–150.7	–38.4	0.012	–45.8	14.8	5.5013	80.9	–14.9	0.180	–100.3
17.0	–19.2	0.110	–147.8	–37.8	0.013	–52.1	14.8	5.4892	67.9	–14.6	0.186	–97.4
17.5	–21.1	0.088	–138.0	–37.3	0.014	–60.7	14.7	5.4475	54.4	–14.3	0.194	–95.6
18.0	–22.1	0.079	–117.7	–36.7	0.015	–69.6	14.7	5.4016	40.5	–13.7	0.206	–95.1
18.5	–20.7	0.092	–96.6	–35.9	0.016	–74.8	14.5	5.3231	26.1	–13.3	0.217	–96.0
19.0	–18.2	0.123	–83.9	–35.4	0.017	–85.0	14.3	5.2168	11.2	–13.0	0.224	–98.0
19.5	–15.4	0.169	–80.3	–35.0	0.018	–95.7	14.0	5.0371	–4.3	–12.9	0.226	–99.4
20.0	–13.0	0.224	–81.8	–34.8	0.018	–105.6	13.7	4.8240	–19.9	–13.0	0.225	–100.9
20.5	–11.1	0.278	–85.7	–34.7	0.018	–114.9	13.2	4.5580	–36.4	–13.3	0.217	–99.8
21.0	–9.6	0.332	–91.2	–34.2	0.020	–126.3	12.5	4.2135	–52.5	–13.8	0.205	–97.5
21.5	–8.3	0.384	–97.7	–34.3	0.019	–137.2	11.7	3.8489	–68.9	–14.0	0.199	–90.2
22.0	–7.3	0.432	–284.7	–34.2	0.020	–328.3	10.8	3.4671	–85.5	–13.4	0.214	–80.1

Notes:

1. Data obtained from on–wafer measurements.

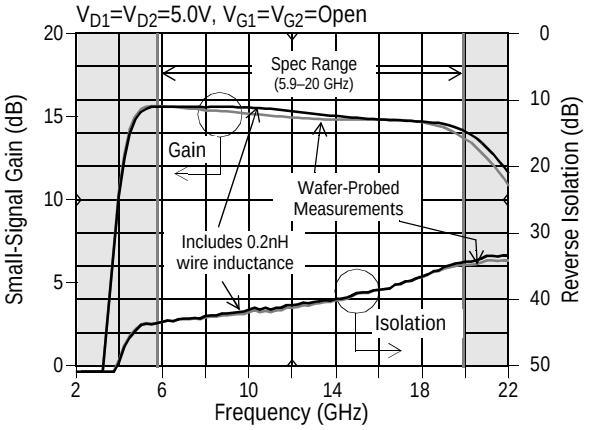


Figure 4.
Effects of Input / Output Bond Wire Inductance on Gain and Isolation[1]

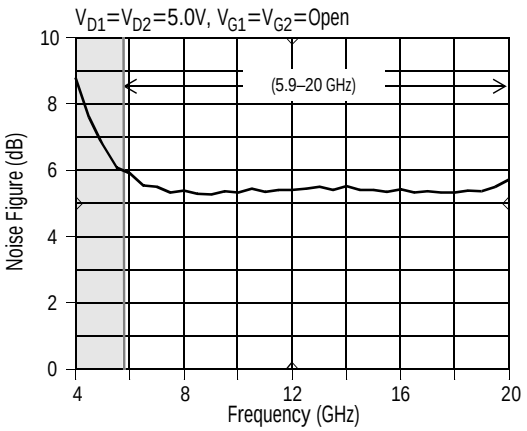


Figure 5.
Noise Figure versus Frequency[2]

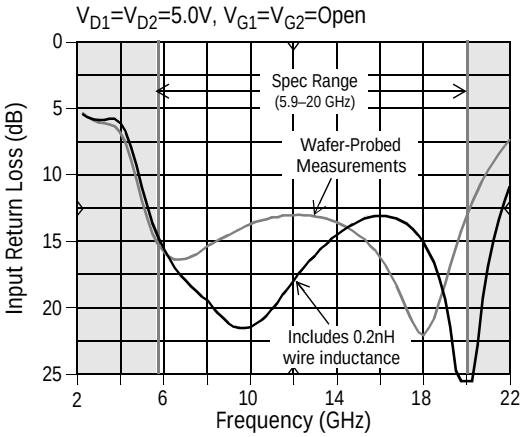


Figure 6.
Effects of Input / Output Bond Wire Inductance on Input Return Loss[1]

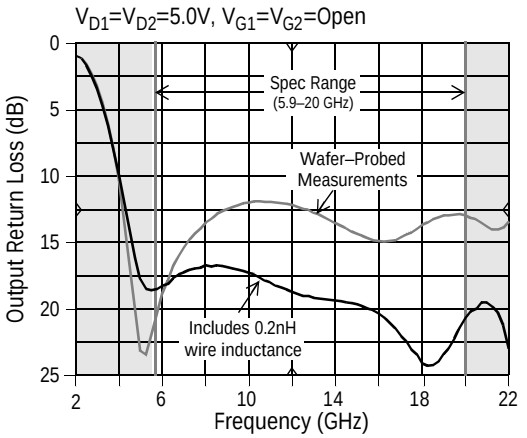


Figure 7.
Effects of Input / Output Bond Wire Inductance on Output Return Loss[1]

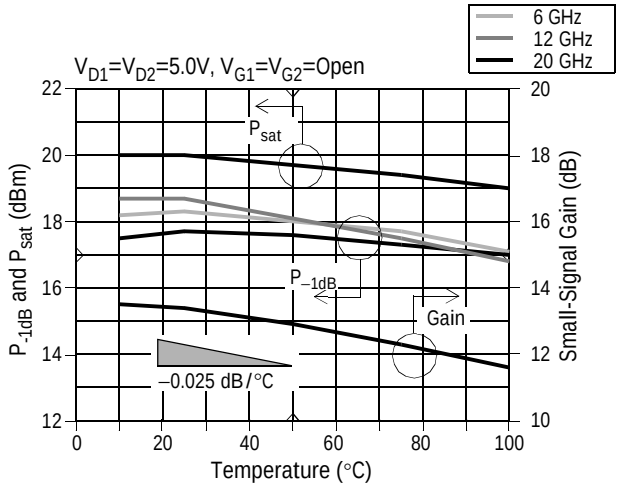


Figure 8.
Power and Gain versus Backside Temperature[2]

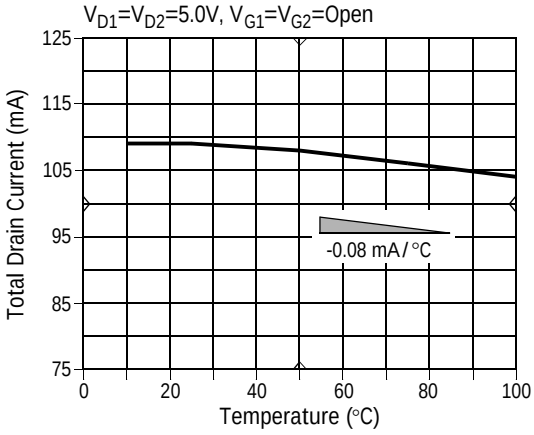


Figure 9.
Drain Current versus Backside Temperature[2]

[1]Effect of 0.2nH inductance in the RF input and RF output bond wires is modeled from measured wafer–probe tests calibrated at the pads of the MMIC device.

[2]Wafer–probed measurements.

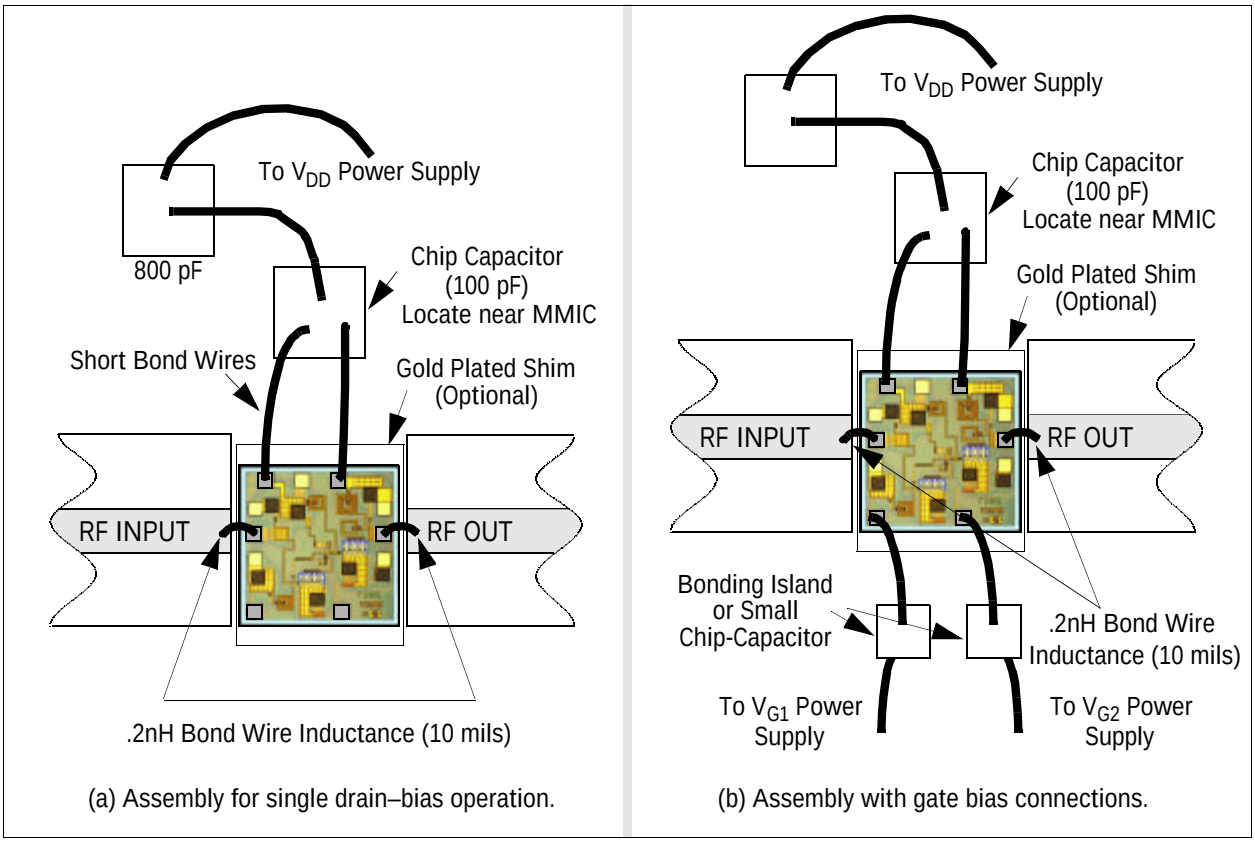


Figure 10.
Assembly Diagrams

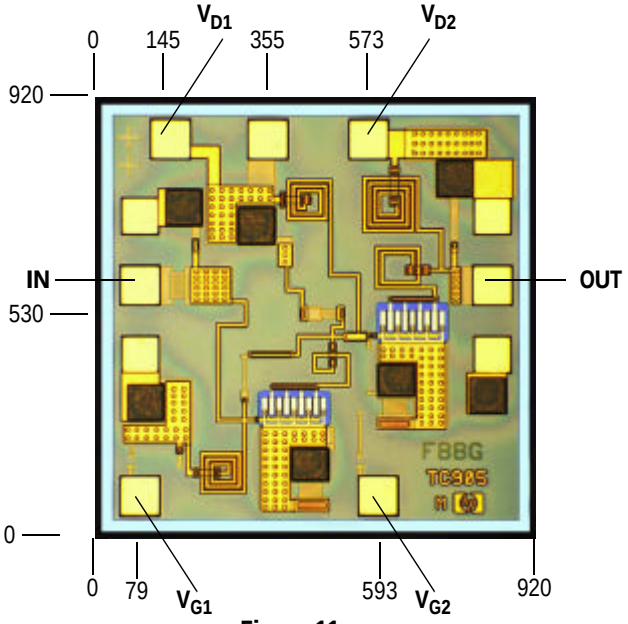


Figure 11.
Bonding Pad Positions
(Dimensions are in micrometers)

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Agilent Technologies' sales representative.

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